THE SPECIFICATION:

Paragraph bridging pages 3 and 4, please replace with the following:

Fig. 3 is a circuit diagram showing a configuration of a ~~substrate voltage generating~~ level shift circuit according to a second embodiment of the voltage generating circuit of the present invention.

Paragraph bridging pages 5 and 6, please replace with the following:

The level shift circuit 101 is connected between a first power supply node to which a power supply voltage VDD (first power voltage) is supplied, and the output node OUTvbb. An input signal in.101 (first input signal) is supplied to an input terminal IN of the level shift circuit 101 and an input signal /in.101 (second input signal), which is complementary to the input signal in.101, is supplied to an input terminal /IN. The input signal in.101 and the input signal /in.101 are signals each having an amplitude ranging from a power supply voltage VDD to a power supply voltage VSS (hereinafter referred to as VDD/VSS). For example, the power supply voltage VDD is set to 3.0 V and the power supply voltage VSS is set to OV. An output signal out 101 is outputted from an output terminal OUT of the level shift circuit 101. The output signal out.101 a signal having the amplitude ranging from a power supply voltage VDD to a substrate voltage VBB (hereinafter referred to as VDD/VBB). The substrate voltage VBB is a negative voltage which is lower than the power supply voltage VSS. For example, the substrate voltage VBB is set to ~~-1.5 V~~ -1.5V.

Page 8, paragraph 2, please replace with the following:

An output signal osc of an oscillator circuit (not ~~sown~~ shown) is supplied to a first input terminal of a NAND 1 circuit, a power down signal pump is supplied to a second input terminal thereof, and an output signal of an inverter circuit INV6 is supplied to a third input terminal thereof. The NAND 1 circuit outputs an inverting signal of a logical product (AND). An output signal of the ~~NADN~~ NAND 1 circuit is a signal having an amplitude of VDD/VSS.

Page 8, paragraph 3, please replace with the following:

An output signal /osc of an oscillator circuit (not ~~sown~~ shown) is supplied to a first input terminal of a NAND 2 circuit, the power down signal pump is supplied to a second input terminal thereof, and an output signal of an inverter circuit INV5 is supplied to a third input terminal thereof. The output signal /osc is a signal having a phase opposite to the output signal osc supplied to the first input terminal of the NAND 1 circuit. The NAND 2 outputs an inverting signal of the logical product (AND). An output signal of the ~~NADN~~ NAND 2 is a signal having an amplitude of VDD/VSS.

Page 12, paragraph 2, please replace with the following:

An operation of the level shift circuit 101 is described next with reference to Fig. 2. When the input signal in.101 of "L" (~~substrate voltage~~ ~~VBB~~ power supply voltage VSS) is supplied to the input terminal IN, the PMOS transistor P1 turns ON. At this time, since the substrate voltage VBB is supplied to the source of the NMOS transistor N1, the NMOS transistor N1 does not turn ON completely and functions as a resistance element. Further, since the thickness of the gate oxide film of the NMOS transistor N1 is set to a thickness thicker than those of the NMOS transistors N3 and N4, the NMOS transistor N1 has relatively high resistance value at this time period.

Page 16, paragraph 3, please replace with the following:

Fig. 3 is a circuit diagram showing the configuration of the ~~substrate voltage generating~~ level shift circuit according to the second embodiment of the substrate voltage generating circuit of the invention.

Paragraph bridging pages 16-18, please replace in its entirety:

The level shift circuit of the substrate voltage generating circuit of the second embodiment of the invention comprises PMOS transistors P31 (first transistor) and P32 (second transistor), and NMOS transistors N31 (third transistor), N32 (fourth transistor), N33 (fifth transistor) and N34 (sixth transistor). The PMOS transistor P31 has a gate to which the input signal in.101 (first input signal) is supplied, a source connected to the first power supply node to which the power supply voltage VDD is supplied, and a drain connected to a node n31 (first node). The PMOS transistor P32 has a gate to which the input signal /in.101 (second input signal) having a phase opposite to the input signal in.101 is supplied, a source connected to the ~~second~~ first power supply node to which the power supply voltage VDD is supplied, and a drain connected to the node ~~n31~~ n32. The NMOS transistor N31 has a gate connected to the node ~~n31~~ n32, a source connected to the NMOS transistor N33, and a drain connected to the drain of the PMOS transistor P31. The NMOS transistor N32 has a gate connected to the drain of the PMOS transistor P31, a source connected to the NMOS transistor N34, and a drain connected to the output terminal OUT. The NMOS transistor N33 has a gate to which the input signal in.101 is supplied, a source connected to the output node OUT.vbb, and a drain connected to the source of the NMOS transistor N31. The NMOS transistor N34 has a gate to which the input signal /in.101 is supplied, a source connected to the output node OUT.vbb, and a drain connected to the source of the NMOS transistor N32. The node ~~n31~~ n32 is connected to the output terminal OUT.

Paragraph bridging pages 18-20, please replace in its entirety.

Described first is an operation in the case where the input signal in.101 of "L" (power supply voltage VSS) is supplied to the input terminal IN, and the input signal /in.101 of "H" (power supply voltage VDD) is supplied to the input terminal /IN. The PMOS transistor P31 turns ON in response to the input signal in.101 of "L" (power supply voltage VSS). At this time, since the substrate voltage VBB is supplied to the source of the NMOS transistor N33, the NMOS transistor N33 does not turn ON completely and functions as a resistance element. Further, since the thickness of the gate oxide film of the NMOS transistor N33 is set to a thickness thicker than those of the NMOS transistors N31 and N32, the NMOS transistor N33 has relatively high resistance value at this time period. Further, the PMOS transistor P32

turns OFF and the NMOS transistor N34 turns ON in response to the input signal /in.101 of "H" (power supply voltage VDD). Since the NMOS transistor N33 functions as the resistance element, the power supply voltage VDD is instantaneously supplied to the gate of the NMOS transistor N32, and hence the NMOS transistor N32 turns ON. This means that the level shift circuit 101 operates rapidly. Since the NMOS transistor N32 turns ON, the ~~the~~ voltage of the output terminal OUT goes "L", the substrate voltage VBB. Since the voltage of the output terminal OUT goes "L", i.e. the substrate voltage VBB, the NMOS transistor N31 turns OFF. In such a manner, the substrate voltage VBB is outputted from the output terminal OUT of the level shift circuit.